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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,469	09/26/2003	Shin-Ichi Hashimoto	514802002700	9722

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EXAMINER	
QUASH, ANTHONY G	

ART UNIT	PAPER NUMBER
2881	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,469	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Anthony Quash	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' amendment has overcome the objection to claim 3 listed in the previous office action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,11,12 are rejected under 35 U.S.C. 102(b) as being anticipated by Okamoto [314]. As per claims 1,11, and 12, Okamoto [314] discloses an electron beam exposure method and apparatus for exposing a wafer by an electron beam comprising, an electron beam generating section for generating the electron beam, a deflector for deflecting the electron beam, a deflection control section for outputting a deflection control signal for causing the deflector to deflect the electron beam, and a control signal storage section for storing a value of the electron deflection control signal output from the deflection control section. See Okamoto [314] abstract, figs. 1-3,11, col. 1 lines 35-40, col. 3 lines 40-65, col. 4 lines 5-10, 15-62, col. 5 lines 1-15, col. 7 lines 15-40, col. 9 lines 30-60, col. 10 lines 3-40, and col. 14 lines 10-15, 25-40.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2,4-6,9-10,13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto [314]. As per claim 2, Okamoto [314] teaches all aspects of the claim except for explicitly stating that the control signal storage section and deflector being monolithically integrated on a semiconductor substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the control signal storage section and deflector be monolithically integrated on a semiconductor substrate, since it has been held that making formerly separable structures into an integral structure involves only routine skill in the art.

As per claim 4, Okamoto [314] teaches all aspects of the claim except for explicitly teaching a switch for switching whether the deflection control signal is to be supplied to the control signal storage section. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a switch for switching whether the deflection control signal is to be supplied to the control signal storage section in order to all one to make adjustment to the deflection without wasting unnecessary computer memory.

As per claim 5, Okamoto [314] teaches all aspects of the claim except for explicitly stating that the deflection control signal output the deflection control signal in

binary form to the control storage signal when the switch supplies the deflection control signal to the control signal storage section, and the deflection control section output the deflection control signal, which is an analog signal when the switch does not supply the deflection control signal to the control signal storage section. It would have been obvious to one of ordinary skill in the art to have the deflection control signal output the deflection control signal in binary form to the control storage signal when the switch supplies the deflection control signal to the control signal storage section, and the deflection control section output the deflection control signal, which is an analog signal when the switch does not supply the deflection control signal to the control signal storage section in order to reduce the amount of memory used when transmitting the signal the control storage section (computer) since it is well known that computers operate in binary, and machinery operates in analog.

As per claims 6,9-10, Okamoto [314] teaches all aspects of the claim except for explicitly stating the deflection control section supply a plurality of deflection control signals to the plurality of deflectors and the control signal storage section store values of the plurality of deflection control signals in parallel, and output them to the deflection control section in series. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have the deflection control section supply a plurality of deflection control signals to the plurality of deflectors and the control signal storage section store values of the plurality of deflection control signals in parallel, and output them to the deflection control section in order to allow easier identification of

electrodes that are damaged, and to insure that the beams are deflected in the proper sequence.

As per claim 13, Okamoto [314] teaches all aspects of the claim except for explicitly stating that the apparatus further comprise a signal line for connecting the deflection control section and the deflector, the signal line including a deflection control signal input terminal on a semiconductor substrate on which the control signal storage section is formed. It is inherent that the apparatus would comprise a signal line for connecting the deflection control section and the deflector, the signal line including a deflection control signal input terminal on a semiconductor substrate on which the control signal storage is formed, since one would have to have a means for conveying the signal from the deflector to an output means in order to aid in the measurement of the deflection signal. In addition, this would also be inherent since one would have to have a means for transmitting the an input signal from an input device to the control deflection section in order to indicated amount that the beam is to be deflected.

As per claim 14, Okamoto [314] teaches all aspects of the claim except for explicitly stating that the apparatus further comprise a signal line for connecting a deflection control section for generating the deflection control signal and the deflector, the signal line including a deflection control signal input terminal on a semiconductor substrate on which the control signal storage section is formed. It is inherent that the apparatus would comprise a signal line for connecting the deflection control section for generating the deflection control signal and the deflector, the signal line including a deflection control signal input terminal on a semiconductor substrate on which the

control signal storage section is formed, since one would have to have a means for conveying the signal from the deflector to an output means in order to aid in the measurement of the deflection signal. In addition, this would also be inherent since one would have to have a means for transmitting the an input signal from an input device to the control deflection section in order to indicated amount that the beam is to be deflected.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto [314] in view of Yasuda [597]. As per claim 7, Okamoto [314] teaches all aspects of the claim except for explicitly stating that the deflection control section further output a clock signal, the control signal storage section outputs a value of deflection control signal according to the clock signal. However, Yamada [597] does teach the deflection control section further output a clock signal, the control signal storage section outputs a value of deflection control signal according to the clock signal. See Yasuda [597] abstract, figs. 3-6, column 4, col. 7 lines 60-69, col. 9 lines 1-15, 50-66, col. 10 lines 20-69, and col. 11 lines 4-11, and 28-35. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have the deflection control section further output a clock signal, the control signal storage section output a value of deflection control signal according to the clock signal in order to generate a signal to control deflection, blanking and pattern data memory as taught in Yasuda [597].

As per claim 8, Yasuda [597] teaches the control signal storage section comprising a shift register including a plurality of flip-flops provide corresponding to the

plurality of deflectors, the flip-slops storing thereon values of the corresponding deflection control signals. See Yasuda [597] abstract, figs. 3-6, column 4, col. 7 lines 60-69, col. 9 lines 1-15, 50-66, col. 10 lines 20-69, and col. 11 lines 4-11, and 28-35.

Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto [314] in view of Hamaguchi [624]. As per claim 3, Okamoto [314] teaches all aspects of the claim except for explicitly stating a plurality of deflecting electrodes being provided in the edges of the aperture for receiving the plurality of deflection control signals, respectively, and the plurality of deflecting electrodes being electrically isolated from one another. However, Hamaguchi [624] does teach a plurality of deflecting electrodes being provided in the edges of the aperture for receiving the plurality of deflection control signals, respectively, and the plurality of deflecting electrodes being electrically isolated from one another. See Hamaguchi [624] abstract, figs. 1-33, and col. 3 lines 5-30. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have a plurality of deflecting electrodes being provided in the edges of the aperture for receiving the plurality of deflection control signals, respectively, and the plurality of deflecting electrodes being electrically isolated from one another in order to all independent deflection of the beams as taught in Hamaguchi [624].

Response to Arguments

Applicant's arguments filed 7/12/04 have been fully considered but they are not persuasive. With respect to the applicants' arguments concerning Okamoto [5,557,314] not teaching a storage section for storing the deflection control signal, it is

the examiner's view that Okamoto [5,557,314] does. This point is made evident from Okamoto [5,557,314] fig. 1, column 4, col. 7 lines 30-40, column 10, col. 13 line 60 – col. 14 line 10-40, col. 16 lines 10-25. Here it teaches the control computer (21) with contains a data storage section and a processing unit (24) of the control I/O section 2, drawing data from buffer memory. From here it is obvious that all input and outputs (including deflection control signals) are stored. In addition, fig. 17 clearly shows deflector (14) being connected to memory (75) thereby storing output deflection control signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent No. 4,437,008 to Matsuda et al is considered pertinent to the applicants' disclosure. Matsuda [4,437,008] is considered pertinent due to its discussion on an electron beam control system.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Quash whose telephone number is (571)-272-2480. The examiner can normally be reached on Monday thru Friday 9 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R. Lee can be reached on (571)-272-2477. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Quash

10/4/04

JOHN R. LEE
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